Venue and Registration Details

Venue
The courses are organized in Virginia Tech’s Research Center, 900 N Glebe Road, Arlington, Virginia. The venue is conveniently located and can be reached by car, as well as metro. Nearby hotels are the Westin Arlington Gateway and the Holliday Inn Ballston. These hotels will provide a reduced rate to course participants; follow the links on the course website (http://rijndael.ece.vt.edu/cescacourse).

Registration
The cost per course is $1800. This includes two-and-a-half days of lecture, lecture materials, and coffee breaks. Course fee reductions apply to participants who register for multiple courses, and for groups. Participants can register through the Virginia Tech Continuing and Professional Education website (http://www.cpe.vt.edu/reg/cesca/). Registration deadline is June 11, 2012.

Questions can be directed to Patrick Schaumont (schaum@vt.edu).
In collaboration with the Continuing and Professional Education organization at Virginia Tech, CESCA is bringing a series of short, two-and-a-half-day courses on contemporary topics in electronic design. The courses are taught by CESCA faculty, and will be offered at Virginia Tech’s Research Center in Arlington, Virginia. The courses are open to both industry practitioners and academics.

**Hardware Security: Building Tamper-resistant Cryptography**

Date: June 18-20, 2012  
Instructor: P. Schaumont

Hardware Security: Building Tamper-Resistant Cryptography describes hardware design techniques for security-critical operations, such as data encryption or key generation. The widespread use of programmable hardware platforms and reconfigurable hardware has made secure hardware design a viable, trustworthy alternative to software. Secure hardware is particularly useful when high-performance, low-power operation, and/or trustworthiness of a design is critical. The two-and-a-half day course on Hardware Security introduces the key concepts in secure hardware design, including the major technologies for cryptographic implementations, and design techniques for trustworthiness. The lectures combine theory with practical hands-on sessions in a computer lab.

**Hunting for Software Bugs: Software Correctness and Security**

Date: June 20-22, 2012  
Instructors: S. Shukla and M. Hsiao

Hunting for Software Bugs: Software Correctness and Security is a course designed to teach in two and a half days of intensive sessions about formal and informal methods for bug hunting – both to assure correctness, and for ensuring that unintended security compromises are not present in your software. With the advent of the ubiquitous computing - apps, servers behind clouds, services and middlewares have been dominating our lives. Financial to national power grid, all need to run secure and bug-free software.

This course introduces the key concepts in software assurance - from the standpoint of functional correctness as well as security. Covers formal and informal methods for test and modeling, secure programming, and techniques to look for security bugs. The lectures combine theory with practical hands-on sessions in a computer lab.

**Small-scale Energy Harvesting: Principles, Practices and Future Trends**

Date: June 25-27, 2012  
Instructor: D. S. Ha

Harvesting small scale energy from otherwise wasted ambient energy sources has attracted immense interest for various battery-powered devices such as wireless sensor nodes, implant devices, variable traffic signs, and wireless light switches. The power level required for those applications may range from microwatts to a few watts, and the energy scavenged from ambient sources may be able to recharge or even eliminate the battery to power up those devices perpetually. This course reviews principles of energy harvesting and practices for small scale energy harvesters.

**Hardware/Software Codesign on Platform FPGA’s**

Date: June 27-29, 2012  
Instructor: P. Schaumont

Hardware/Software Codesign on Platform FPGA’s describes design techniques for mapping complex, system-on-chip-like designs on Field Programmable Gate Arrays. Such designs typically contain one or more embedded processors, along with a range of custom-designed hardware modules. The two-and-a-half day course on Hardware/Software Codesign introduces the key ideas in hardware/software codesign, including system-modeling, analysis of system-level descriptions, system-level architecture customization and optimization. Participants will familiarize themselves with a modern FPGA design flow based on Altera chips. Participants will receive course lecture materials, the design examples from the hands-on sessions, and the FPGA design kit. Developed recently. Recent research efforts in energy harvesting, commercial products available in the market, and future trends are also covered. The course includes hands-on experiments with an energy harvesting kit. Participants will receive course lecture materials, the energy harvesting kit, and the design examples from the hands-on sessions.